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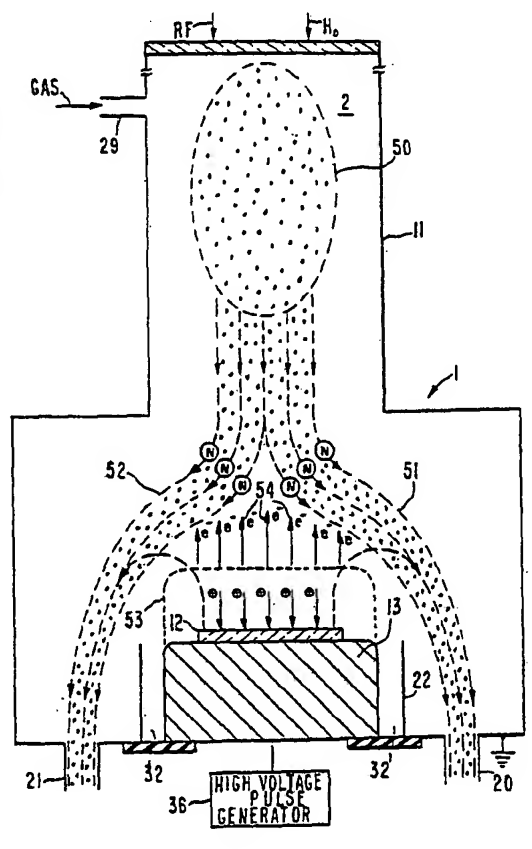
(54) Title: PLASMA IMPLANTATION PROCESS AND EQUIPMENT

(57) Abstract

A method and apparatus is provided for ion implantation for large dose, low energy work which does not immerse the target wafer (12) in the plasma (50) and which obtains good sheet resistance uniformity, high production rate and good under 100 nm shallow junction depth control.



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PLASMA IMPLANTATION PROCESS AND EQUIPMENT

Field of the Invention

This invention relates to the field of semiconductor processing and particularly to the field of doping of semiconductors by ion implantation.

Background of the Invention

Materials called semiconductor are the basis of most of modern electronic devices. Semiconductor materials, such as silicon, have a crystalline structure in which each atom is tightly bound to its neighbor such that the material is a very poor conductor of electricity because none of the carriers of electricity are mobile. Some electrons can become conductors if they acquire sufficient energy to break free. The conductivity of a pure semiconductor is called the intrinsic conductivity, but the material is not useful as an electronic device in that form. A small amount of certain types of impurity are needed to be added into its crystal lattice. Even an extremely small amount of such impurities will provide a tremendous increase in the number of current carriers. Usually the impurity selected is an atom of the same size as the semiconductor atom having a different number of electrons in its outer or valence band so as to result in a chemically bonded structure where the unbonded electron or hole can move around in the structure with very little energy expenditure. This process of adding an impurity has typically been called "doping". Early doping was accomplished by simultaneously placing a plurality of semiconductor wafers in a high temperature diffusion furnace into which has been added gas containing dopant which was diffused into the semiconductor. This process worked well for most early so called discrete transistors.

However, when it became important to increase the number and decrease the size of each transistor on a given piece of silicon, it became important to gain much more precise control over the spatial distribution and concentration of impurities added to the semiconductors than was possible employing the diffusion process. At this stage, a device known as an ion implanter became the usual tool for adding the necessary impurity to the crystal. These implanter devices are complex large devices capable of very precise control of a dopant ion beam which beam was typically scanned to uniformly cover the entire wafer surface.

In recent years, as semiconductor technology has continued to evolve, it has become recognized that the standard ion implanter has certain limitations in application where a low energy beam (under 10KV) is required, especially where the requirement is for high dose and production rate (wafer throughput) for the processing apparatus. A method known as Plasma Immersion Ion Implantation (PI^3) is being considered for this application. Using PI^3 apparatus, a high ion density (10^{10} - 10^{11} cm^{-3}) plasma is able to be generated. A substrate near the plasma is negatively biased causing positive ions to be accelerated toward the substrate and implanted therein. The dose rate can be high, i.e., 10^{16} cm^{-2} s^{-1}, and large samples can be implanted quickly without any scanning.

Prior PI^3 work is described by N.W. Cheung, "Plasma Immersion Ion Implantation for ULSI Processing", Nuclear Instruments and Methods in Physics Research, 1355 (1991), pp. 811-820. This system locates the target within the plasma in the center of the plasma chamber and away from the chamber walls.

The object of our invention is to provide an improved implantation apparatus with the uniformity of scanning implantation but with the simplicity of PI^3.

A further object is to provide simple implantation apparatus with shallow junction capability, having high throughput, as well as better uniformity and control of implant.

Summary of the Invention

The present invention provides a configuration which applies a pulsed uniform electric field over one surface of a large area target electrode so that a large cross section ion beam is available. To accomplish this goal, the target electrode upon which the substrate workpiece is to be mounted is placed on the downstream chamber wall as opposed to being immersed in the plasma, and a unipolar, variable pulse width high voltage is applied to the target. This configuration also permits a symmetrical plurality of vacuum pumping ports to be placed completely around the target to facilitate symmetrical removal of reaction products and neutral species during implantation.

Also provided is a ground shielding which is symmetrically placed close to and distributed around the sides of the target electrode, so that secondary plasma formation is eliminated.

Description of Drawing

FIG. 1 is a schematic representation of a cross section of a portion of our inventive implanter.

FIG. 2 is a cross section of an embodiment of our invention.

FIG. 3A is a bottom view of our implanter showing the symmetry of the vacuum ports.

FIG. 3B is section BB side view of FIG 3A exhaust manifold.

FIG. 4A, 4B and 4C are alternate embodiments of workpiece and electrode configurations.

Detailed Description of the Invention

With reference to FIG. 1, the operation of our ion implantation apparatus is explained schematically. We cause a plasma 50 generated in region 2 to flow into chamber 1 where the semiconductor wafer 12 is to be treated. There are several different plasma regions within our device during operation. In the region depicted by the dashed line 50, at low pressures, electrons are induced to undergo electron cyclotron resonance (ECR) which creates a plasma in the ion source region 11. ECR will be more fully described subsequently. The plasma is essentially electrically neutral since it consists of approximately equal number of electrons and positively charged species. Only a small percentage of the atoms in the plasma are ionized at any given instant. This plasma has a plasma potential of approximately +20 volts. Under the influence of the pressure differential from vacuum pumping of ports 20, 21, 20a and 21a, and the pressure from mass flow controller introducing gases into the inlet 29 near the top of the plasma source, the charged and the neutral species flow from the source 2 into process chamber 1 toward the highly conductive target electrode 13. As this flow moves toward the target 13, some flow divides and moves along equal conductance paths toward the symmetrically located vacuum port exhausts 21 and 20 and 20a and 21a in the bottom wall of the process chamber 1. The flow rate is adjusted so that some of these flowing gases flow around and toward the exhaust ports and provide a steady state refreshing of the dopant species.

When a high voltage pulse, i.e. -3KV, is provided to electrode 13 from generator 36, the electrons 54 in the charged gas in the close vicinity of the electrode 13 are repelled first, because they are lighter. This leaves a positively charged sheath of ions in the immediate vicinity 53 of the target electrode. This sheath extends to a distance of 1 to 3 cm above the target electrode 13. The positive ions in this region 53 are accelerated by the large area negative potential of the target along the straight field lines perpendicular to the planar face of

the electrode 13. Since the workpiece wafer 12 is situated between the gases and the electrode 13, the positive ions impact and implant into the wafer.

All of the exhaust ports are preferably connected as shown in bottom views, FIGS. 3A and 3B, to a centrally located manifold 37 in order to have a uniform and symmetrical pressure gradient in the vicinity of the target electrode for uniform distribution of plasma components and the reaction products.

Very high voltage gradients exist in the gap 32 between the side wall of the target electrode 13 and the cylindrical ground shield 22. This gap 32 must be large enough so that an arc is not struck in this space and so that the region is cleanable. It is preferable to round the corners of the target 13 and shield 22 near the mouth of the gap 32 to avoid field emission and spurious arcing. Our embodiment will not arc below 6KV DC. Also, the gap 32 must be narrow enough so that ions cannot be trapped in the gaps to sustain a plasma when the accelerating voltage pulse is supplied to the target 13. This gap distance is related to the chamber pressure and should be less than the order of the mean free path for the ion involved at the pressure employed. In our configuration, the gap 32 is on the order of 0.125 inches.

The preferred embodiment of our invention is more fully described with reference to FIG. 2. A standard microwave generator 5 is coupled to the ECR plasma source 2 via waveguide 7 containing an RF tuner 6 such as a stub tuner. The microwaves enter into the plasma source through RF window quartz disk 8. To prevent etching of quartz window 9, an alumina layer 9 could be coated on disk 8 or it could be part of the alumina chamber liner 10, as shown. There are four symmetrical dopant species gas inlet lines 29 (only 2 shown) which introduce the dopant through mass flow controller 30 from a gas source 31. When BF_3 is the source gas, sputtering of contaminants

from the stainless steel walls of the plasma chamber may occur which will introduce contaminant ions into the implant.

Magnet coils 3 and 4 are shown surrounding the plasma source 2 and provide the uniform strong axial fixed magnetic field necessary to sustain electron cyclotron resonance in the chamber 2. An electron in motion in a magnetic field is acted upon by the field to produce force on the electron at right angles to the direction of motion of the electron. As a result, an electron entering a fixed magnetic field will follow a curved path. The radius of curvature is an inverse function of the intensity of the magnetic field. The frequency of electron rotation, w, is expressed as $w=2.8\ X10^6B$ cycles/sec where B is in gauss. This is known as the electron cyclotron resonance frequency. We have designed our ECR plasma generator to employ a magnetic field of 875 gauss and the corresponding cyclotron frequency of 2.45 GHz.

The liner 10 is preferably made from alumina but could be made from any material which does not contain elements which should not be co-implanted. The liner material could be made of a material that is resistant to sputtering or chemical etching by the plasma species. In the case of processing with BF_3, resistant materials include oxides (i.e. alumina), nitrides (i.e., boron nitride or silicon nitride) or carbides (i.e., silicon carbide). Alternatively, the liner could be of a sacrificial material which has measurable etch rates in the presence of the plasma species, but does not contribute undesirable impurities which could be co-implanted. Examples of sacrificial materials include carbon (i.e., graphite, diamond) or poly-crystalline silicon. The plasma source chamber could be coated with films of liner materials which could be applied by plasma spraying, CVD, sputtering or evaporation. Alternatively, the plasma source chamber walls could be protected by a separate piece of material composed entirely of or coated with the desired liner material.

Magnet 19 is a coil which may be used to assist in canceling the magnetic fields in the vicinity of the target electrode to improve plasma ion density uniformity at electrode/wafer interface. Chamber 1 is an axially symmetrical structure with the target electrode 13 mounted to the wall of the chamber opposite from the mouth of plasma source 2. A wafer load lock 26 having its own vacuum pump port 24, can receive up to 25 wafers at once through door 25. Slit valve 27 permits the loading and unloading of the chamber by a transfer arm (not shown) without requirement for pumping down from atmosphere each time a new wafer is introduced in the chamber. It is believed that our system will be able to treat 30 six-inch wafers per hour when fully automated for doping time per wafer of 1 minute. During wafer doping only the four ports 20, 21, 20a and 21a are pumped. At other times the chamber can be pumped through high conductance side port 38 at greater speed to provide a lower base pressure. During loading of a wafer the pressure is below 1 X 10^{-6} torr in the chamber. We find that this helps eliminate deposition on the wafer and coimplantation of contaminating elements.

The target electrode 13 is electrically isolated from the chamber walls by a dielectric ring vacuum seal 23 and mechanically clamped (not shown) to the chamber wall. The ground shield wall 22 surrounding the target restricts secondary plasma formed in the gap 32. Accordingly, our wafer temperatures are typically able to be maintained below 60°C without any active cooling of the target electrode. This low temperature operation is a feature of our invention since final implantation junction depth is very much a function of the processing temperatures. Additionally, it is frequently required to implant through photoresist layers or photoresist masks. Temperatures must be below 100°C to avoid degradation of these layers. We have discovered that we can routinely make devices having final junction depths less than 100nm after rapid thermal processing at 1050°C activation of 10 seconds.

Connected to our electrode 13 via conductor 14 is high voltage pulse generator 16 having a variable duty cycle control. By controlling both the amplitude and pulse duty cycle, we can influence the energy distribution of the ions to be implanted. Our equipment employed for this purpose is standard, such as Velonex® Model 350 generator which also provides the ability to adjust the DC bias of the wafer. At this time, we have discovered that the optimum process conditions for BF_3 is a chamber pressure during implantation of 1.0 mtorr, a microwave power of 800 watts, a pulse voltage of negative 3.5 KV with a pulse length of 12μ seconds and a pulse period R, of 1msec with a total processing time of 60 seconds. This corresponds to a duty cycle of 1.2%. This set of parameters results in a 90nm junction depth p-type layer after a rapid thermal anneal step. Our sheet resistance is approximately 200 Ω/sq. The 1-sigma uniformity of this sheet resistance on a 150mm diameter silicon wafer is less than 3%.

Viable implantation can be carried out over the following range of conditions. The flow rate of BF_3 gas can be varied between 4 to 50 SCCM giving pressures of 0.3-2.0 mtorr and the microwave power varied from 550 to 1400 W. Pulse voltages can be varied from 1-30μ seconds at voltages from 1-5KV. Pulse repetition rate can be varied from DC to 10,000 Hz.

Our chambers can be oriented with the wafer facing up, down, or sideways with respect to gravity. We believe that the quality of the finished product is independent of the gravity orientation of the wafer during implantation so long as the gas flows in a straight line from the source region to the wafer and passes around the wafer as it is being pumped out.

We have elected to use ECR as the plasma generating technique. Other types of remote plasma generation providing high density, low plasma potential such as inductively coupled plasma generation, helicon or hollow cathode sources could also be employed.

With reference to FIG. 2, we have determined that ion bombardment of the aluminum target electrode 13 in the region of the periphery 39 of the wafer 12 could be responsible for the introduction of contamination of the wafer being implanted. The embodiments of FIG. 4A, 4B and 4C show other configurations of the target 13 which improve or overcome this difficulty.

With reference to FIG. 4A, we show a shortening of the target electrode 13a so that its periphery exactly matches the periphery of the overlying target 12. Obviously this configuration will reduce the extent of the target 13a which is directly bombarded by ions. FIG. 4B illustrates our preferred target electrode embodiment which is a configuration where the target electrode 13b has a diameter which is considerably smaller than the diameter of the wafer 12a. This configuration also avoids contamination by shielding the electrode from direct ion bombardment.

Another target electrode configuration is shown in FIG. 4C. In this embodiment, the target electrode 13c has a very much larger planar surface area 43 than the frontal surface area of the wafer 44. If wafer 12 is a silicon wafer, then the passivation layer 40 would preferably be a silicon wafer of larger diameter than wafer 12 in order to minimize contamination from direct ion bombardment of the target electrode. The wafer 12 may simply be held by gravity on the top surface of the wafer 40 or by use of a vacuum chuck. To improve the heat transfer across wafer 40, its surfaces top and bottom should be very smooth. The temperature of the wafer 12 is not normally a problem because of the lower implantation energy employed in our invention than in comparison to raster scanning implantation techniques. However, it may be desirable to employ active temperature control of the wafer for certain applications. This could be achieved with backside gas coupling between the wafer and a temperature controlled electrode. In this configuration, a positive wafer clamp would be required.

It is understood that the present invention is not limited to the particular embodiments set forth herein but embraces all such modified forms which come within the scope of the following claims.

We Claim:

1. In an ion implanter including a plasma ion source and an ion accelerating voltage source connected to a target to cause ions to move, in operation, towards said target, THE IMPROVEMENT COMPRISING:

said target being a target electrode;

a workpiece processing chamber;

said plasma ion source being mounted to said workpiece processing chamber, said workpiece processing chamber having said target electrode directly and fixedly mounted thereto and electrically isolated therefrom, said target electrode having a planar front surface facing into said workpiece processing chamber; and

said ion accelerating voltage source being a variable duty cycle high voltage unipolar pulse generator having a oscillator period R and a pulse width W, where the duty cycle W/R is selectable.

2. In the ion implanter of claim 1 wherein the said target electrode is a right circular cylinder and wherein all points on the side wall of said right circular cylinder are electrically isolated from said workpiece process chamber by the same electrical resistance, said workpiece processing chamber having a cylindrical metallic shield substantially surrounding the said sides walls of said target electrode wherein said cylindrical metallic shield is at a distance from said target electrode side walls which is less than the mean free path of the ions in said workpiece processing chamber.

3. In the ion implanter of claim 2, wherein said plasma ion source is an ECR plasma source including a microwave generator, a cylindrical resonance chamber coupled to said microwave generator by a waveguide through an RF window, said cylindrical resonance

chamber being lined with a material on all surfaces including said RF window which liner material is selected from a group of materials which will not contaminate the workpiece.

4. In the ion implanter of claim 3, wherein said liner material is selected from the group of dielectrics including alumina, graphite, polysilicon, boron nitride, silicon nitride, silicon carbide, diamond, or carbon.

5. In the ion implanter of claim 4 wherein the surface of said target electrode opposite said planar surface of said target is in direct contact with ambient temperature environment for passive cooling.

6. A semiconductor ion implantation apparatus for treating a wafer comprising:

an ECR ion source having a cylindrical configuration, a first diameter and an axis;

a process chamber being cylindrically shaped and having a second diameter and an axis;

said ECR ion source axis being coextensive with said process chamber axis and said ECR source opening into said process chamber;

a target electrode having a side wall and a planar top and bottom surface, said target electrode being a cylindrical disk of highly conductive metal, the axis of said cylindrical disk being coaxial with said process chamber axis; said process chamber having a cylindrical shield surrounding said side wall of said cylindrical target electrode in close proximity thereto; and said planar top surface of said target electrode being passivated so that it does not introduce contaminants into said process chamber during operation.

7. The apparatus of claim 6 wherein said target electrode is passivated by placing a passivating layer of material on top of said target electrode for supporting said wafer to be treated.

8. The apparatus of claim 7 wherein said passivating layer of material is a semiconductor wafer having a diameter equal to or larger than the entire said top surface area of said target electrode to minimize bombardment of said target electrode surface by ions.

9. The apparatus of claim 8 wherein said passivating layer diameter is large enough to also overlap said process chamber cylindrical shield to preclude bombardment of said side walls of said target electrode.

10. The apparatus of claim 9 wherein said passivating layer semiconductor material is selected from the same semiconductor material of said wafer to be processed.

11. The apparatus of claim 6 wherein said processing chamber includes a plurality of vacuum ports substantially equally and symmetrically spaced from and around said electrode target to maintain, in operation, an isopressure region on the order of 1 mtorr in the said processing chamber near said electrode target.

12. Ion implantation apparatus for treating a wafer comprising;

(a) downstream plasma generating means including a chamber to generate said plasma and means to flow said plasma to a processing region;

(b) ion accelerating means in said processing region to simultaneously draw a large cross section beam of ions from said

flowing plasma, said large cross section being on the order of 100 mm or larger including;

a target electrode, said target electrode having a large area flat surface for supporting said wafer workpiece placed at a distance removed from said plasma generating chamber, said target electrode being located adjacent said flowing plasma; and

high voltage pulse generating means connected to said target electrode, and means to apply said high voltage pulses to said target electrode to cause said large cross section beam to impact a workpiece wafer substantially perpendicularly to the surface of the wafer across the entire front surface of said wafer.

13. The ion implantation apparatus of claim 12 wherein said high voltage pulse generating means includes means for selecting the duty cycle of said high voltage pulses.

14. The ion implantation apparatus of claim 13 wherein said target electrode is passivated.

15. The ion implantation apparatus of claim 14 wherein said passivated target electrode comprises said wafer material having an area equal to or larger than said large area front surface which is placed above and in contact with said large area front surface of said target electrode.

16. A method for implanting ions into a semiconductor wafer comprising,

placing said wafer on a large area planar surface target, said target being made from a highly conductive material;

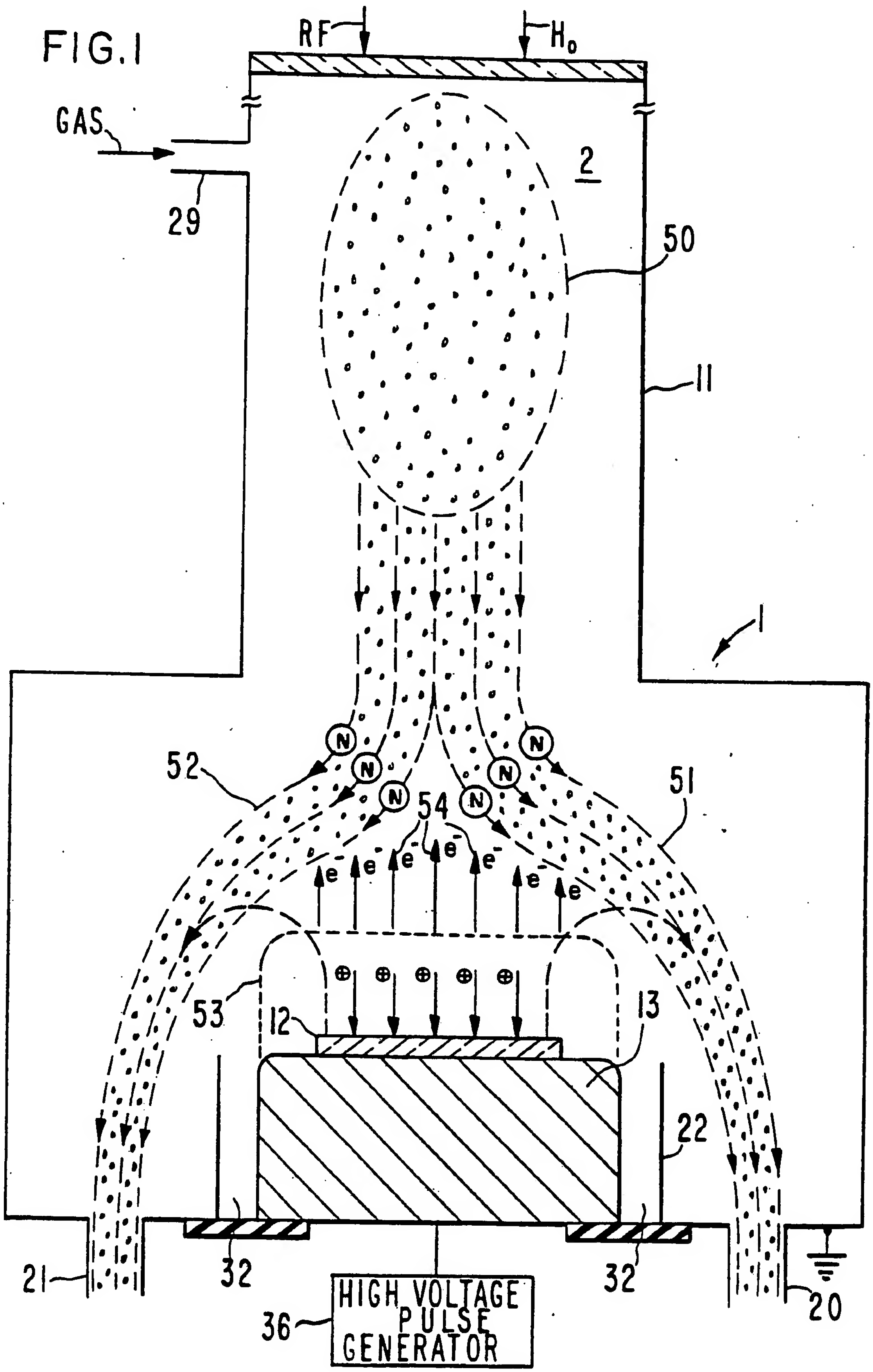
forming, in a nearby region, an ionized plasma containing a dopant ion, at pressures near 1 mtorr;

locating said target outside of said ion forming region and flowing said ionized plasma uniformly toward and around said target; and

applying a sequence of high voltage pulses to said target to cause said dopant ions to be drawn from said flowing plasma and to be accelerated along unidirectional electric field lines created by said planar surface target toward said target and implanting into said wafer only on the surface of said wafer removed from said target.

17. The method of claim 14 wherein the step of applying said sequence of high voltages pulses includes selecting the duty cycle of said pulses to control the energy distribution of ions.

FIG.1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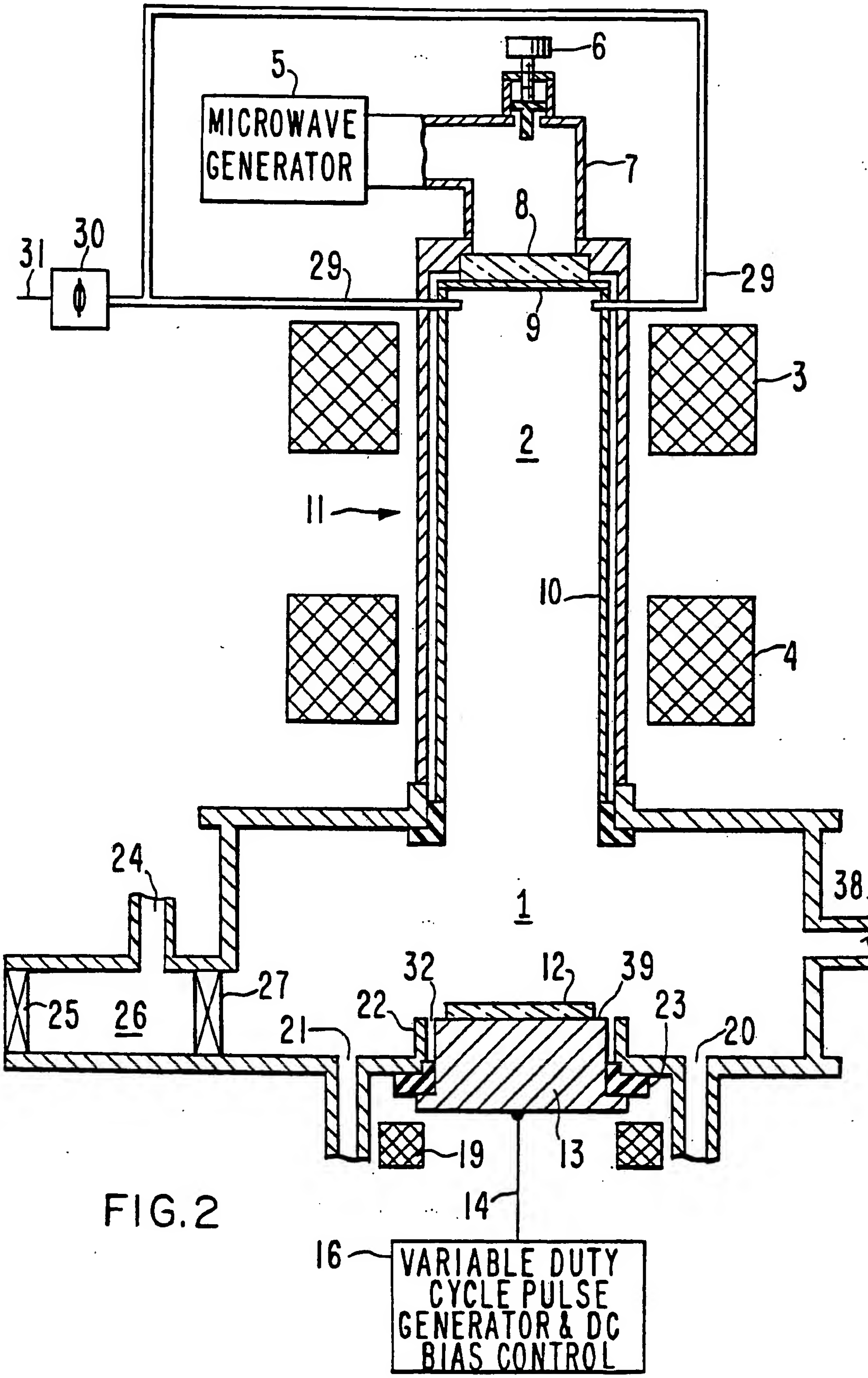


FIG.2

SUBSTITUTE SHEET

FIG.3A

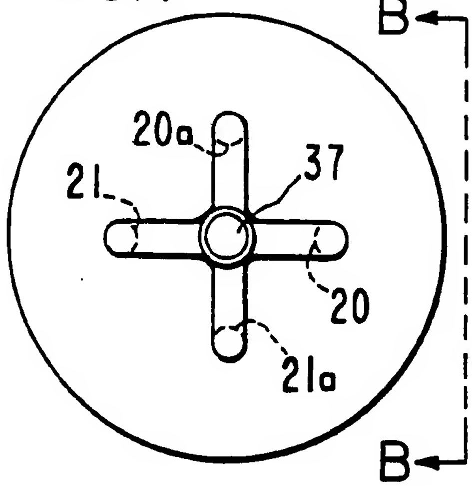


FIG.3B

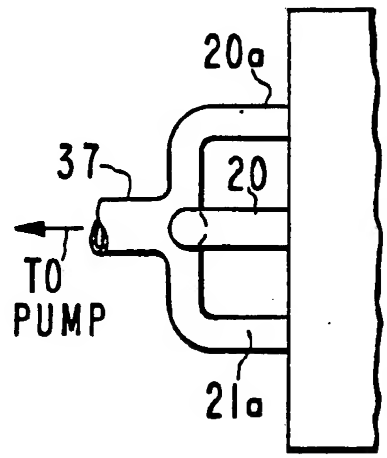


FIG.4A

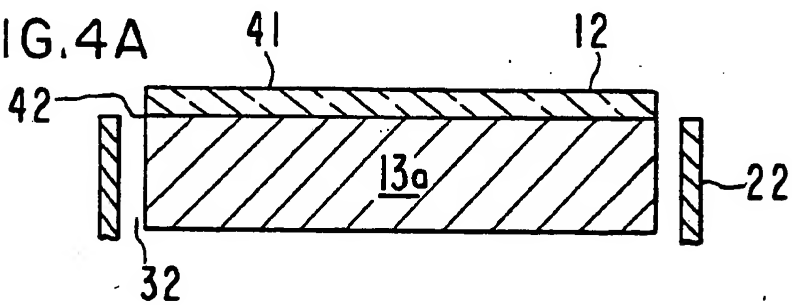


FIG.4B

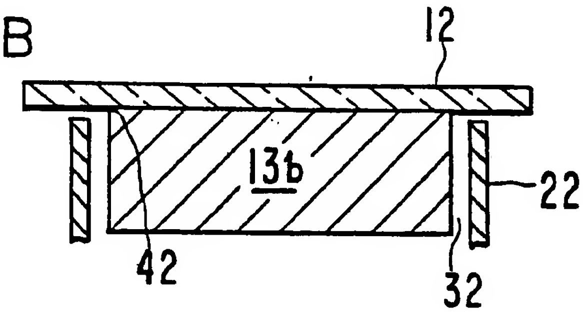
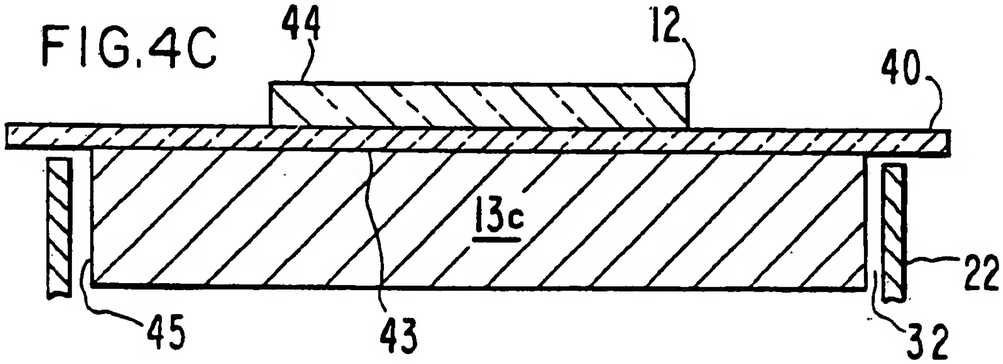


FIG.4C



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/01788

A. CLASSIFICATION OF SUBJECT MATTER

IPC(5) :C23C 14/48
US CL :427/523,575; 204/298.05; 118/723,728
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 427/523, 575; 204/298.05; 118/723, 723

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	N. Cheung, "Plasma immersion ion implantation for ULSI processing", Nuclear Inst. and Methods in physics Research, B55 (1991) p. 811-820. See figures 4 and 11.	1,12-13 and 16-17
X	X. Qian et al., "Plasma Immersion Ion Implantation for VLSI Fabrication", Memorandum No. UCB/ERL M90/84, 13 September 1990. See entire document.	1,12-13 and 16-17
Y	US,A, 4,399,016 (Tsulada et al.) 16 August 1983, see figures 1-2.	2-5
Y	US,A, 4,732,761 (Machida et al.) 22 March 1988, see figures 1-3.	2-5

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US93/01788

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US,A, 4,384,918 (Abe) 24 May 1983, see figures 1-4.	6-11 and 14-15
Y	US,A, 4,897,171 (Ohmi) 30 January 1990, see figure 1.	6-11 and 14-15